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Títol de la tesi
PREDICTION OF THE IMPACT OF SUBSTRATE COUPLED SWITCHING NOISE ON FREQUENCY SYNTHESIZERS, USING HIGH-LEVEL ANALYSIS AND MODELS

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As the trend to miniaturization, power consumption reduction and higher data rates in integrated circuits continues, circuit designers are pushed to integrate every time more and more electronic systems co-existing in single silicon dies. As those systems are integrated closer it is more likely that they interact and perturb each other. One particularly troublesome interaction from the point of view of the modeling in modern CMOS integrated circuits is the one that happens between the large digital circuits and the sensitive RF circuits. Misestimating this effect can result in economical losses as it is necessary to redesign and implement the circuit again. Frequency synthesizers are particularly sensitive to the noise coming from digital circuits. The noise coupled through the substrate or through other physical path, can degrade the synthesizer's output phase and this certainly undesired effect that can be hardly corrected. Modeling this effect involves different challenging aspects, the first is to estimate the noise produced by a large digital circuit, the second is to obtain a model of the propagation path (in our case restricted to the substrate) and the last is to simulate the RF circuit under the noise effects.

This work is divided in two parts; in the first part the generation of the noise by large digital circuits and the noise propagation through the substrate are studied. A linear time invariant macromodel composed by only current sources, resistors and capacitors is used to simplify the complexity of the digital circuit transistor level model. This work introduces a method to estimate the minimum error by this simplification. It also proposes a method to reduce the complexity of the substrate model and it is verified with excellent results using a circuit simulator. The complete model including the noise macromodel of a large digital circuit together with the substrate model is verified against measurements. The first part concludes with an explanation of the possible sources of errors in the experiment proposed to verify the model.

The second section deals with the modeling of the supply noise to phase noise conversion in a PLL. This complements the first part as we studied how the noise that is produced by the digital circuits in the PLL interconnections becomes phase noise in the PLL output. A complete frequency synthesizer for the Bluetooth wireless communication standard composed of a PLL is designed and it is measured as a test case. We propose a general method to calculate the noise conversion in the PLL. For this method the conversion gain for the different components of the PLL is calculated using a Linear-Time-Variant circuit simulator, the overall contribution of every component of the PLL is added assuming that the loop behaves linearly and taking care of the different phases among the different noise contributions. This method makes possible to calculate the overall phase noise degradation due to the noise in the supplies without the necessity of having to simulate the complete PLL with the noise sources, a task that can take long time or even be unfeasible. The model also gives insight over the relevance of the different noise contributions. The work closes with a set of measurements of the Bluetooth synthesizer that shows the same tendency predicted by the proposed model.

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